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PATENT

IN THE U.S. PATENT & TRADEMARK OFFICE

Applicant: CHIN-LONG CHEN	:	GROUP ART UNIT:
Serial No.: TBD	:	Examiner:
Filed: Herewith	:	October 9, 2001
Title: BLOCK-SERIAL FINITE	:	Lawrence D. Cutter
FIELD MULTIPLIERS	:	IBM Corporation, IP Law Dept.
	:	M/S P386, 2455 South Road
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INFORMATION DISCLOSURE STATEMENT


Assistant Commissioner for Patents  
Washington, D. C. 20231

Sir:

Listed on the accompanying form PTO-1449 are documents that are being submitted for consideration under 37 CFR 1.97 and 1.98. Copies of the documents are enclosed.

Song and Parhi discuss a similar approach but do not employ intermediate processing mod  $p(x)$ . As a result, their storage requirements are higher.

RESPECTFULLY SUBMITTED,

  
Lawrence D. Cutter,  
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POU920000039US1

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Express Mail Label No.: ET089965542US  
Date of Deposit: October 9 2001

I hereby certify that this correspondence is being deposited with the United States Postal Service, on the date indicated above, as Express Mail Post Office to Addressee Service under 37 CFR 1.10 and is addressed to Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

  
Susan L. Phelps

October 9, 2001  
Date of Signature



<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>	ATTY DOCKET NO. <b>POU920000039US1</b>	SERIAL NO. <b>TBD</b>
	APPLICANT(S) <b>C. L. Chen</b> <span style="float: right;"><b>Express Mail #ET089965542US</b></span>	
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**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

**FOREIGN PATENT DOCUMENTS**

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*

c	Mastrovito, E., <i>VLSI Designs for Multiplication over Finite Fields GF(2m)</i> , Lecture Notes in Computer Science, Vol. 357, Berlin: Springer-Verlag, March, 1989, pp. 297-309.
d	Peterson, W., <i>Error-Correcting Codes</i> , The MIT Press, 1961,

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					YES	NO

**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		e	Song et al., Low-Energy Digit-Serial/Parallel Finite Field Multipliers, Journal of VLSI Signal Processing 19, Kluwer Academic Publishers, 1998, pp. 150-166.